Amendments to the Claims:

The listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1. (Currently amended) A method for dynamically configuring a redundant area of a page associated with a physical block of a non-volatile memory of a memory system, the method comprising:

determining whether a predetermined metric value associated with performance of the non-volatile memory meets a predetermined criterion by checking one or more metric values stored in the non-volatile memory;

~~determining whether~~ storing at least one byte in ~~associated with~~ the redundant area when the predetermined metric meets the predetermined criterion ~~is to be altered~~, the at least one byte ~~including~~ corresponding to an error correction code (ECC) ~~information associated with~~ used by a first ECC algorithm to check for errors in the page;

altering the at least one byte when the predetermined metric fails to meet the predetermined criterion, ~~responsive to determining that the at least one byte is to be altered,~~ wherein ~~altering~~ the at least one altered byte corresponds to an ECC used by a second ECC algorithm to check for errors in the page, where the first ECC algorithm and the second ECC algorithm have differing computational costs. ~~includes altering the at least one byte to include ECC information associated with a second ECC algorithm.~~

2. (Previously presented) The method of claim 1 wherein the first ECC algorithm is a one-bit ECC algorithm.

3. (Currently amended) The method of claim 2, wherein the at least one byte includes ECC information associated with the first ECC algorithm, and includes:

approximately three bytes ~~arranged to be~~ used to correct an error associated with a first group of bytes of a data area of the page,

approximately three bytes ~~arranged to be~~ used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes ~~arranged to be~~ used to correct an error associated with the redundant area.

4. (Original) The method of claim 2 wherein the second ECC algorithm is a 2-symbol ECC algorithm.

5. (Currently amended) The method of claim 4 wherein the at least one byte includes ECC information associated with the second ECC algorithm, and includes:

approximately five bytes ~~arranged to be~~ used to correct at least one error associated with the data area of the page,

approximately three bytes ~~arranged to be~~ used to correct at least one error associated with the redundant area.

6. (Currently amended) The method of claim 1 ~~further including:~~

~~obtaining at least one bit which is arranged to~~ where the predetermined metric value is stored in the redundant area and indicates a number of times the physical block has been erased ~~from the redundant area~~, wherein the predetermined metric value is compared to the ~~determining whether the at least one byte is to be altered includes determining whether the at least one bit is approximately equal to a~~ predetermined criterion. ~~value.~~

7. (Currently amended) The method of claim [[1]] 6 wherein the predetermined metric value includes a single ~~at least one~~ bit ~~includes information associated with~~ corresponding to an erase count of the physical block, where a state of the single bit is used to compare an erase count with the predetermined criterion, and where the predetermined criterion includes a threshold value corresponding to a number of times that the physical block has been erased.

8. (Currently amended) The method of claim [[1]] 7 wherein the single bit is a digit of an erase counter used to determine ~~at least one byte associated with the redundant area~~

~~is to be altered includes determining whether~~ a number of erase cycles undergone by the physical block ~~has reached a threshold level~~.

9. (Canceled)

10. (Original) The method of claim 1 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

Claims 11. – 20. (Canceled)

21. (Currently amended) A memory system comprising:

a non-volatile memory, the non-volatile memory including a physical block, wherein the physical block has a page with a data area and a redundant area;

means for determining whether a predetermined metric associated with performance of the non-volatile memory meets a predetermined criterion by checking one or more metric values stored in the non-volatile memory;

means for storing at least one byte in the redundant area when the predetermined metric meets the predetermined criterion, the at least one byte corresponding to an error correction code (ECC) used with a first ECC algorithm to check for errors in the page; and

means for altering the at least one byte when the predetermined metric fails to meet the predetermined criterion, wherein the at least one altered byte corresponds to an ECC used with a second ECC algorithm to check for errors in the page, where the first ECC algorithm and the second ECC algorithm have differing computational costs.

~~means for determining whether at least one byte associated with the redundant area is to be altered, the at least one byte including error correction code (ECC) information associated with a first ECC algorithm;~~

~~means for altering the at least one byte responsive to determining that the at least one byte is to be altered, wherein altering the at least one byte includes altering the at least one byte to include ECC information associated with a second ECC algorithm.~~

22. (Currently amended) The memory system of claim 21 wherein the first ECC algorithm is a 1-bit ECC algorithm and wherein the at least one byte includes ECC information used by ~~associated with~~ the first ECC algorithm, and includes:

approximately three bytes ~~arranged to be~~ used to correct an error associated with a first group of bytes of a data area of the page,

approximately three bytes ~~arranged to be~~ used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes ~~arranged to be~~ used to correct an error associated with the redundant area.

23. (Currently amended) The memory system of claim 22 wherein the second ECC algorithm is a 2-symbol ECC algorithm, and wherein the at least one byte includes ECC information used by ~~associated with~~ the second ECC algorithm, and includes:

approximately five bytes ~~arranged to be~~ used to correct at least one error associated with the data area of the page, and

approximately three bytes ~~arranged to be~~ used to correct at least one error associated with the redundant area.

24. (Currently amended) The memory system of claim 21 further including:

means for obtaining a value from the redundant area that corresponds to ~~at least one bit which is arranged to indicate~~ a number of times the physical block has been erased, and where the predetermined metric comprises a number of times the physical block has been erased. ~~from the redundant area, wherein the means for determining whether the at least one byte is to be altered include means for determining whether the at least one bit is approximately equal to a predetermined value~~.

25. (Canceled)

26. (Original) The memory system of claim 21 wherein the non-volatile memory system is one of an embedded system, a Smart Media card, a Compact Flash card, a Secure Digital Card, and a MultiMedia card.

27. (Currently amended) A method for processing a page associated with a physical block of a non-volatile memory of a memory system, the method comprising:

determining whether at least one byte associated with a first error correction code (ECC) algorithm is to be altered ~~to be associated~~ for association with a second ECC algorithm based on whether a predetermined metric associated with performance of the non-volatile that is stored in a redundant area of the page meets a predetermined criterion, the at least one byte being stored in a redundant area associated with the page; and

dynamically configuring the redundant area in response to the predetermined metric meeting or failing to meet the predetermined criterion ~~responsive to determining that the at least one byte is to be altered~~ such that the at least one byte is altered to be associated with the second ECC algorithm.

28. (Original) The method of claim 27 wherein the first ECC algorithm is a 1-bit ECC algorithm and the second ECC algorithm is a 2-symbol ECC algorithm.

29. (Currently amended) The method of claim 28 wherein the at least one byte associated with the first ECC algorithm includes:

approximately three bytes ~~arranged to be~~ used to correct an error associated with a first group of byte of a data area of the page,

approximately three bytes ~~arranged to be~~ used to correct an error associated with a second group of bytes of the data area, and

approximately two bytes arranged to be used to correct an error associated with the redundant area.

30. (Currently amended) The method of claim 28 wherein the at least one byte is altered to be associated with the second ECC algorithm, and includes:

approximately five bytes ~~arranged to be~~ used to correct at least one error associated with the data area of the page, and

approximately three bytes ~~arranged to be~~ used to correct at least one error associated with the redundant area.

31. (Canceled)

32. (Previously presented) The method of claim [[31]] 27 wherein the predetermined metric comprises an indication of ~~indicator is arranged to indicate~~ a number of times the physical block has been erased~~, and wherein whether the indicator is approximately equal to a predetermined value, the indicator indicates the at least one byte is to be altered~~.

33. (Currently amended) A method for dynamically configuring a redundant area of a page associated with a physical block of a non-volatile memory of a memory system, the method comprising:

determining whether a set of bits in the redundant area is to be altered based on whether a predetermined metric associated with performance of the non-volatile memory meets a predetermined criterion, where the redundant area includes information corresponding to the predetermined metric, the set of bits including error correction code (ECC) information associated with a first ECC algorithm, wherein [[a]] the set of bits are substantially grouped in a first configuration for use by the first ECC algorithm; and

altering [[a]] the set of bits responsive to determining that the predetermined metric meets the predetermined criterion ~~that the set of bits is to be altered~~, wherein ~~altering the set of bits includes altering~~ the set of bits are altered to include ECC information associated with a second ECC algorithm, and substantially grouped ~~and grouping a set of bits~~ in a second configuration for use by the second ECC algorithm.

34. (Original) The method of claim 33 wherein the set of bits includes approximately eighth bytes and the first configuration includes a first subset of approximately three bytes, a second subset of approximately three bytes, and a third subset of approximately two bytes.

35. (Original) The method of claim 34 wherein the second configuration includes a first grouping of approximately five bytes and a second grouping of approximately three bytes.

36. (Original) The method of claim 33 wherein the first ECC algorithm is a 1-bit ECC algorithm and the second ECC algorithm is a 2-symbol ECC algorithm.

37. (Previously presented) The method of claim 33 wherein the predetermined metric comprises a number of times that the physical block has been erased. ~~determining whether the set of bits is to be altered is based on whether includes determining whether an indicator stored in the redundant area indicates that the set of bits is to be altered.~~

38. (Canceled)

39. (New) A memory system comprising:

a non-volatile memory, the non-volatile memory including a physical block, where the physical block includes a page with a data area and a redundant area; and

a memory manager operable to

access a metric parameter value from the redundant area, where the metric parameter value corresponds to performance of the non-volatile memory,

compare the metric parameter value with a predetermined criterion,

store a first error correction code (ECC) in the redundant area of the page, where the first ECC is used by a first ECC algorithm when the metric parameter value meets the predetermined criterion, and

store a second ECC in the redundant area of the page, where the second ECC is used by a second ECC algorithm when the metric parameter value fails to meet the predetermined criterion, where the first and second ECC algorithms have different computational costs.

40. (New) The memory system of claim 39, where the predetermined criterion comprises a number of times that the physical block has been erased.

41. (New) The memory system of claim 40, where the first ECC algorithm has a lower computational cost than the second ECC algorithm, and where the second ECC algorithm is used when the number of times that the physical block has been erased exceeds a predetermined number.

42. (New) The memory system of claim 41, where the memory manager comprises a counter that tracks the number of times that the physical block has been erased.

43. (New) The memory system of claim 39, where the memory manager further operates to organize bits in the redundant area in a first configuration when the first ECC algorithm is employed, and to organize bits in the redundant area in a second configuration when the second ECC algorithm is employed.

44. (New) A memory system comprising:

a non-volatile memory, the non-volatile memory including multiple physical blocks, where each of the physical blocks includes a page with a data area and a redundant area; and

a memory manager operable to

keep track of an average number of times that the multiple physical blocks of the non-volatile memory have been erased,

store a first error correction code (ECC) in the redundant area of a page, where the first ECC is used by a first ECC algorithm when the average number of times that the multiple physical blocks have been erased is less than a predetermined value, and

store a second ECC in the redundant area of the page, where the second ECC is used by a second ECC algorithm when the average number of times that the multiple physical blocks have been erased exceeds the predetermined value, where the first ECC algorithm has a lower computational cost than the second ECC algorithm.

45. (New) The memory system of claim 44, where the memory manager further operates to organize bits in the redundant area in a first configuration when the first ECC algorithm is employed, and to organize bits in the redundant area in a second configuration when the second ECC algorithm is employed.